**National University**



**of Computer & Emerging Sciences**

**Course Outline of BS (Computer Science) Degree Program --Spring 2020**

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| **Course Title** | | | Digital Logic Design (DLD) | | | **Course Code** | EE227 |
| **Pre-requisite(s)** | | | None | | | **Credit Hrs.** | 3 + 1 |
| **Instructor** | | | Musawar Ali | | | | |
| **Email** | | | musawar.ali@nu.edu.pk **Phone Ext**  113 | | | | |
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| **Text Book (1)** | | | **Title** | Digital Fundamentals | | | |
| **Author** | Thomas L. Floyd | | | |
| **Publisher** | Pearson Education , 10th or 11th Edition | | | |
| **Text Book (2)** | | | **Title** | Digital Design | | | |
| **Author** | M. Morris Mano, Michael Ciletti | | | |
| **Publisher** | Pearson Education , 4th Edition | | | |
| **Ref. Book (1)** | | **Title** | | | Digital Principles and Applications | | |
| **Author** | | | Donald P Leach, Albert Paul Malvino, Goutam Saha | | |
| **Publisher** | | | McGraw Hill Companies, 6th Edition | | |
| **Ref. Book (2)** | | **Title** | | | Digital Systems Principles and Applications | | |
| **Author** | | | Ronald J. Tocci, Neal S. Widmer, Gregory L. Moss | | |
| **Publisher** | | | Pearson Education, 10th Edition | | |
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| **Objective:** | | | The objective of this course is to introduce concept & tools for the design of digital electronics circuits using sequential and combinational | | | | |
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| **Week** | **Course Contents/Topics** | | | | | | **Chapter** |
| 01 | Introduction. Digital Electronics. Digital Principles. Analog Vs. Digital. Basic Logic operations. | | | | | | 1 |
| 02 | Number Systems. Binary to Decimal. Decimal to Binary conversion. Hexadecimal Number system. BCD code. The Byte, Nibble and Word. | | | | | | 2 |
| 03 | Logic Gates, AND OR & NOT Gates, NOR NAND XOR Gates. | | | | | | 3 |
| 04 | Boolean Algebra and logic simplification. DeMorgan’s Theorems. Boolean analysis of Logic circuits. Truth Tables. The Karnaugh Map. | | | | | | 4 |
| 05 | Basic Combinational circuits. Implementing Combinational Logic. Using NAND and NOR Gates. | | | | | | 5 |
| 06 | **Mid Term 1** | | | | | |  |
| 07  &  08 | Basic Adders. Parallel Binary Adders. Ripple v/s Look-Ahead carry adders. Comparators. Decoders. Encoders. Multiplexers. Demultiplexers. | | | | | | 6 |
| 09  &  10 | Latches. Edge-Triggered Flip-Flops. Flip-Flop Operating Characteristics.  Flip-Flop applications. | | | | | | 7 |
| 11 | Asynchronous Counters. Synchronous Counters. Cascaded Counters. Counter Decoding. | | | | | | 8 |
| 12 | **Mid Term 2** | | | | | |  |
| 13  &  14 | Basic Shift Register Operations. Serial In/Serial Out Shift Registers. Serial In/Parallel Out and Parallel In/Parallel Out Shift Registers. Bidirectional Shift Registers. | | | | | | 9 |
| 15  &  16 | Memory Basics, the Random-Access Memory. The Read-only Memory. Programmable ROM. The Flash Memory. Memory Expansion. Special Types of Memories. Magnetic & Optical Storage. | | | | | | 10 |

**Grading Policy:**

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| **Midterm** | 30% |
| **Class Quizzes** | 10% |
| **Assignments/Project/Viva** | 10% |
| **Final Exam** | 50% |
| **Total** | 100% |